AMENDMENTS TO THE CLAIMS

1. (original): A circuit for sensing a logic state of a match line of a content addressable memory (CAM) device, said circuit comprising:

an input adapted to receive a first current signal, which changes based on said logic state of said match line; and

a circuit having a first portion for receiving said first current signal and converting said first current signal to a first voltage signal and a second portion adapted to produce a second voltage output signal based on said first voltage signal.

2. (original): The sensing circuit according to claim 1, wherein said first portion of said circuit includes a transistor connected as a diode.

3. (original): The sensing circuit according to claim 2, wherein said transistor comprises a p-channel transistor.

4. (original): The sensing circuit according to claim 2, wherein said transistor comprise an n-channel transistor.

5. (original): The sensing circuit according to claim 1, wherein said sensing circuit further comprises:

a first transistor having one of a source and a drain coupled to said input and the other of said source and said drain coupled to a first node; and

a second transistor having one of a source and a drain coupled to said output node, the other of said a source and said drain coupled to receive a potential from a first potential source, and a gate coupled to said first potential source.

6. (original): The sensing circuit according to claim 5, wherein said current mirror circuit comprises:

a third transistor having one of a source and a drain coupled to said first node, the other of said source and said drain coupled to a first potential source and a gate coupled to a second node and to said first node; and

a fourth transistor having one of a source and a drain coupled to said first potential source, the other of said source and said drain coupled to an output node, and a gate coupled to said second node.

7. (original): The circuit sensing according to claim 6, wherein said third and said fourth transistors are electrically matched.

8. (original): The sensing circuit according to claim 5, wherein said first potential source comprises a source of ground potential.

9. (original): The sensing circuit according to claim 1, wherein said match line of said CAM device has a plurality of CAM cells coupled thereto.

10. (original): The sensing circuit according to claim 1, wherein said first portion of said circuit includes a transistor coupled to exhibit negative feedback.

11. (original): The sensing circuit according to claim 6, further comprising a fifth transistor for precharging said sensing circuit.

12. (original): The sensing circuit according to claim 6, further comprising a fifth transistor for beginning a sensing operation.

13. (original): A circuit for sensing a logic state of a match line of a content addressable memory (CAM) device, said circuit comprising:

an input node coupled to said match line and adapted to receive a memory state logic signal;

a precharge device switchingly coupled between said input node and a source of supply voltage;

a first load device switchingly coupled between said input node and a second node;

an input transistor having a gate and one of a source and a drain mutually coupled to said second node, and the other of said source and said drain coupled to a source of ground potential;

an output transistor having one of a source and a drain coupled to said source of ground potential, a gate coupled to said second node and the other of said source and said drain coupled to an output node; and

a sense-enable device coupled in series with a second load device between said source of supply voltage and said output node.

14. (original): The sensing circuit according to claim 13, wherein said a second load device has a gate coupled to a fixed potential source.

15. (original): The sensing circuit according to claim 13, wherein said input transistor is a p-channel transistor.

16. (original): The sensing circuit according to claim 13, wherein said input transistor is a n-channel transistor.

17. (original): The sensing circuit according to claim 13, wherein said input transistor and said output transistor form a mirror.

18. (original): The sensing circuit according to claim 16, wherein said output transistor is an n-channel transistor.

19. (original): A hybrid current-voltage sensing circuit for sensing a match line of a content addressable memory (CAM) device comprising:

at least one CAM cell coupled to said match line;

a precharge circuit coupled to a supply voltage, said precharge circuit precharging a signal on said match line;

a load circuit coupled to said match line for applying a load to said precharged match line signal;

a mirror having a first portion and a second portion, said first portion coupled to said load circuit; and

a sense enable circuit coupled to said supply voltage for enabling a sensing operation, said sense enable circuit coupled to said second portion of said mirror, said second portion of said mirror having an output corresponding to a state of said match line.

20. (original): The sensing circuit according to claim 19, wherein said sensing circuit comprises:

a first transistor having one of a source and a drain coupled to an input and the other of said source and said drain coupled to a first node; and

a second transistor having one of source and a drain coupled to said output node, the other of said source and said drain coupled to receive a potential from a second potential source, and a gate coupled to said second potential source.

21. (original): The sensing circuit according to claim 20, wherein said current mirror circuit comprises:

a third transistor having one of a source and a drain coupled to said first node, the other of said source and said drain coupled to a first potential source and a gate coupled to a second node and to said first node; and

a fourth transistor having one of a source and a drain coupled to said first potential source, the other of said source and said drain coupled to an output node, and a gate coupled to said second node.

22. (original): The sensing circuit according to claim 21, wherein said third transistor and said fourth transistor are electrically matched.

23. (original): A content addressable memory (CAM) device comprising:

at least one CAM cell coupled to a match line;

a sensing circuit for sensing a logic state of said match line, said sensing circuit comprising:

an input adapted to receive a first current signal, which changes based on a logic state of said match line; and

a circuit having a first portion for receiving said first current signal and converting said first current signal to a first voltage signal and a second portion

adapted to produce a second voltage output signal based on said first voltage signal and convert said second voltage signal into a third voltage signal.

24. (currently amended): A content addressable memory (CAM) device comprising:

at least one CAM cell coupled to a match line;

a sensing circuit for sensing a logic state of ~~a~~ said match line, said sensing circuit comprising:

an input node coupled to said match line and adapted to receive a memory state logic signal;

a precharge device switchingly coupled between said input node and a source of supply voltage;

a first load device switchingly coupled between said input node and a second node;

an input transistor having a gate and one of a source and a drain mutually coupled to said second node, and the other of said source and said drain coupled to a source of ground potential;

an output transistor having one of a source and a drain coupled to said source of ground potential, a gate coupled to said second node and the other of said source and said drain coupled to an output node; and

a sense-enable device coupled in series with a second load device between said source of supply voltage and said output node.

25. (original): A content addressable memory (CAM) device comprising:

at least one CAM cell coupled to a match line;

a sensing circuit for sensing a logic state of said match line, said sensing circuit comprising:

a precharge circuit coupled to a supply voltage;

a load circuit coupled to said match line;

a current mirror having a first portion and a second portion, said first portion coupled to said load circuit; and

a sense-enable circuit coupled to said supply voltage for enabling a sensing operation, said sense-enable circuit coupled to said second portion of said current mirror, said second portion of said current mirror having an output corresponding to a state of said match line.

26. (original): A processing system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for operating said CAM device, said apparatus further comprising:

at least one CAM cell coupled to a match line;

a sensing circuit for sensing a logic state of said match line, said sensing circuit comprising:

an input adapted to receive a first current signal, which changes based on a logic state of said match line; and

a circuit having a first portion for receiving said first current signal and converting said first current signal to a first voltage signal and a second portion adapted to produce a second voltage output signal based on said first voltage signal.

27. (original): A processing system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for operating said CAM device, said apparatus further comprising:

at least one CAM cell coupled to a match line;

a sensing circuit for sensing a logic state of said match line, said sensing circuit comprising:

an input node coupled to said match line and adapted to receive a memory state logic signal;

a precharge device switchingly coupled between said input node and a source of supply voltage;

a first load device switchingly coupled between said input node and a second node;

an input transistor having a gate and one of a source and a drain mutually coupled to said second node, and the other of said source and said drain coupled to a source of ground potential;

an output transistor having one of a source and a drain coupled to said source of ground potential, a gate coupled to said second node and the other of said source and said drain coupled to an output node; and

a sense-enable device coupled in series with a second load device between said source of supply voltage and said output node.

28. (original): A processing system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for operating said CAM device, said apparatus further comprising:

at least one CAM cell coupled to a match line;

a sensing circuit for sensing a logic state of said match line, said sensing circuit comprising:

a precharge circuit coupled to a supply voltage;

a load circuit coupled to said match line;

a mirror having a first portion and a second portion, said first portion coupled to said load circuit; and

a sense-enable circuit coupled to said supply voltage for enabling a sensing operation, said sense-enable circuit coupled to said second portion of said current mirror, said second portion of said current mirror having an output corresponding to a state of said match line.

29. (original): A method for sensing a state of a memory circuit comprising:

receiving a first current signal at an input node, said first current signal corresponding to a logic state of said memory circuit;

converting said first current signal into a second voltage signal; and

converting said second voltage signal into a third voltage signal.

30. (original): The method according to claim 29, wherein said memory circuit comprises a content addressable memory (CAM) device and said input node is coupled to a match line of said CAM device.

31. (original): A method of sensing a voltage to determine a state of a content accessible memory (CAM) device comprising:

precharging said match line;

applying a load to a match line;

sensing a current affected by a logic state of said match line;

producing a first voltage value; and

producing and outputting a second voltage value from said first voltage value.

AMENDMENTS TO THE DRAWINGS

The attached drawing sheets include changes to FIGS. 1-3, 5 and 6 as described in the "Remarks" section of this amendment. The attached sheets replace the originally filed sheets containing FIGS. 1-3, 5 and 6.

Attachments: Five replacement sheets containing FIGS. 1-3, 5 and 6.